IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): ~~A semiconductor device~~ An MISFET comprising:

an n-type silicon carbide substrate of a high impurity concentration;

an n-type silicon carbide layer of a low impurity concentration disposed on the substrate;

a first n-type silicon carbide region of a first impurity concentration disposed on a surface of said n-type silicon carbide layer of the low impurity concentration;

first p-type silicon carbide regions disposed as adjoined to opposite sides of said first n-type silicon carbide region;

a second n-type silicon carbide region of a second impurity concentration disposed selectively from a surface through an interior of said first p-type silicon carbide region at a position separated from said first n-type silicon carbide region;

a wiring of a metal or polycrystalline silicon having a metal or an impurity implanted therein and serving to short-circuit said first p-type silicon carbide ~~region~~ regions to said second n-type silicon carbide region;

a gate electrode disposed in a surface part of each of said first p-type silicon carbide ~~region~~ regions through a gate insulating film; and

a third n-type silicon carbide region of a third impurity concentration formed both between said first n-type silicon carbide region and the first p-type silicon carbide region below said gate electrode and between said second n-type silicon carbide region and the first p-type silicon carbide region below the gate electrode selectively from the surface through the interior of the first p-type silicon carbide region;

all components being individually formed in a vertical DMOS structure.

Claim 2 (Withdrawn): A semiconductor device according to claim 1, wherein said first p-type silicon carbide region has a lower part formed as a second p-type silicon carbide region of a higher impurity concentration than said first p-type silicon carbide region.

Claim 3 (Withdrawn): A semiconductor device according to claim 1, further comprising an n-type silicon carbide region formed selectively from the surface through the interior of the first p-type silicon carbide region below said gate electrode, wherein the n-type silicon carbide region has an impurity concentration sufficient to produce a buried channel region and the buried channel region is formed in a layer thickness 0.2 to 1.0 times a layer thickness of the second n-type silicon carbide region.

Claim 4 (Withdrawn): A semiconductor device according to claim 2, further comprising an n-type silicon carbide region formed selectively from the surface through the interior of the first p-type silicon carbide region below said gate electrode, wherein the n-type silicon carbide region has an impurity concentration sufficient to produce a buried channel region and the buried channel region is formed in a layer thickness 0.2 to 1.0 times a layer thickness of the second n-type silicon carbide region.

Claim 5 (Withdrawn): A semiconductor device according to claim 3 , wherein said buried channel region has an impurity concentration in the range of 5×10^{15} to 1×10^{17} cm^{-3}.

Claim 6 (Previously Presented): A semiconductor device according to claim 1, wherein said gate electrode is formed of aluminum, an aluminum-containing alloy or molybdenum.

Claim 7 (Previously Presented): A semiconductor device according to claim 1, wherein said gate electrode is formed of a p-type polycrystalline silicon having boron implanted therein to a concentration in the range of 1×10^{16} to 1×10^{21} cm^{-3}.

Claim 8 (Previously Presented): A semiconductor device according to claim 1, wherein said gate electrode is formed of an n-type polycrystalline silicon having phosphorus or arsenic implanted therein to a concentration in the range of 1×10^{16} to 1×10^{21} cm^{-3}.

Claim 9 (Previously Presented): A semiconductor device according to claim 1, further comprising a silicide film deposited on said gate electrode, wherein the silicide film is formed of silicon and any one of tungsten, molybdenum and titanium.

Claim 10 (Currently Amended): A semiconductor device according to claim 1, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (11-20) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 11 (Currently Amended): A semiconductor device according to claim 5, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (11-20) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 12 (Currently Amended): A semiconductor device according to claim 6, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (11-20) face of the n-type substrate of a high impurity concentration made of a tetragonal or

rhombohedral silicon carbide single crystal.

Claim 13 (Currently Amended): A semiconductor device according to claim 7, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (11-20) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 14 (Currently Amended): A semiconductor device according to claim 8, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (11-20) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 15 (Currently Amended): A semiconductor device according to claim 9, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (11-20) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 16 (Currently Amended): A semiconductor device according to claim 1, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (000-1) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 17 (Currently Amended): A semiconductor device according to claim 5, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (000-1) face of the n-type substrate of a high impurity concentration made of a tetragonal or

rhombohedral silicon carbide single crystal.

Claim 18 (Currently Amended): A semiconductor device according to claim 6, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (000-1) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 19 (Currently Amended): A semiconductor device according to claim 7, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (000-1) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 20 (Currently Amended): A semiconductor device according to claim 8, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (000-1) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.

Claim 21 (Currently Amended): A semiconductor device according to claim 9, wherein said n-type silicon carbide layer of a low impurity concentration is formed on a (000-1) face of the n-type substrate of a high impurity concentration made of a tetragonal or rhombohedral silicon carbide single crystal.